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Asymmetric carrier transport in flexible interface-type memristor enables artificial synapses with sub-femtojoule energy consumption†

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Flexible and transparent artificial synapses with extremely low energy consumption have potential for use in brain-like neuromorphic electronics. However, most of the transparent materials for flexible memristive artificial synapses were reported to show picojoule-scale high energy consumption with kiloohm-scale low resistance, which limits the scalability for parallel operation. Here, we report on a flexible memristive artificial synapse based on $Cs_3Cu_2I_5$ with energy consumption as low as 10.48 aJ (= 10.48 × 10^{-18} J) μm^{-2} and resistance as high as 243 MΩ for writing pulses. Interface-type resistive switching at the Schottky junction between p-type $Cu_3Cs_2I_5$ and Au is verified, where migration of iodide vacancies and asymmetric carrier transport owing to the effective hole mass is three times heavier than effective electron mass are found to play critical roles in controlling the conductance, leading to high resistance. There was little difference in synaptic weight updates with high linearity and 250 states before and after bending the flexible device. Moreover, the MNIST-based recognition rate of over 90% is maintained upon bending, indicative of a promising candidate for highly efficient flexible artificial synapses.

New concepts

Memristive artificial synapses have been applied to transparent and flexible electronics by exploiting brain-like computing. However, most of the transparent materials for flexible memristive artificial synapses are unsuitable for scalable neuromorphic computing because they show picojoule-scale high energy consumption with kiloohm-scale low resistance. Here we suggest $Cs_3Cu_2I_5$ as a potential candidate for memristive artificial synapses with sub-femto-joule-scale low energy consumption. Resistance as high as 243 MΩ was observed for the writing pulse, which leads to energy consumption of 10.48 aJ (=10.48 × 10^{-18} J) μm^{-2}. The high resistance is attributed to asymmetric carrier transport by p-type $Cs_3Cu_2I_5$ owing to the effective hole mass being three times heavier than effective electron mass. In addition, an MNIST-based recognition rate of over 90% is maintained even upon bending because of the highly bendable characteristic of $Cs_3Cu_2I_5$. This work is expected to provide important insight into material design for energy-efficient and flexible memristive artificial synapses.

Introduction

Artificial neural networks (ANNs) composed of artificial synapses and neurons are suggested to be able to overcome the von Neumann bottleneck by mimicking the information processing of human brains.[1,2] In human brains, 10^{15} synapses and 10^{12} neurons are known to be operated in parallel with only femtojoule (fJ)-scale energy consumption.[3,4] Recently, memristive devices have been proposed for artificial synapses because the metal–insulator–metal (MIM) structure and the redox-based resistive switching mechanism are similar in structure and operation to biological synapses.[4,5] Various materials, such as metal oxides and organic compounds, have been tested as the redox switching medium of memristor devices for artificial synapses and applications of artificial synapses have been extended to transparent and flexible electronics.[6–8] However, most flexible memristor-based artificial synapses exhibit high energy consumption on the picojoule (pJ) scale owing to the relatively low resistance on the kiloohm (kΩ) scale at the given few-volt-scale set/reset voltage and nanosecond time scale, with limited scalability to less than 10^4 arrays for parallel operation.[2,4,6–9] To decrease the energy consumption by three orders of magnitude from pJ to fJ scale along with improvement

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of scalability over 10^6 arrays, memristors require megaohm (MΩ)-scale resistance when writing pulses are applied because the current is the main factor affecting the energy consumption and scalability.[2,9] Thus, active materials that can be switched at high resistance are important for realizing memristor-based artificial synapses with fJ energy consumption and large scalability.

Recently, halide perovskite-based memristors have been reported for artificial synapses, where high resistance states (HRS) occurred on the MΩ scale.[4,10–12] The basis for the large resistance was reported to be due to either the intrinsic properties of halide perovskites or the large potential barrier formed between the electrode and the perovskite.[13–15] Despite the suitability of halide perovskites for artificial synapses, few studies have been reported on perovskite-based flexible and transparent synapses.[16] In addition, most of the studies on perovskite memristors have been performed with lead-based perovskites, which might not be acceptable in the electronics industry.[4,13–15] For this reason, non-Pb-based halide perovskite or pseudo-perovskite materials have been applied to artificial synapses. However, most of the studied materials showed resistance as low as kΩ, which might not be appropriate for sub-fJ energy consumption and parallel operation of 10^6 arrays on the nanoscale.[4,17–19] Thus, it is required to develop technically feasible materials with MΩ-scale resistance for fJ-scale energy consumption transparent, flexible and scalable artificial synapses. To ensure the transparency of the active material, a large bandgap of more than 3 eV is a prerequisite. Recently, $Cs_3Cu_2I_5$ was investigated as a material for blue light-emitting-diodes because of the wide bandgap showing an absorption onset of about 330 nm.[20–23] This indicates that $Cs_3Cu_2I_5$ is optically transparent due to the large optical bandgap of about 3.8 eV. Moreover, a large energy barrier between the $Cs_3Cu_2I_5$ and the metal electrode is expected due to the wide bandgap, which might induce enough resistance to create fJ-scale energy consumption and large scalability. Therefore, we have been motivated to study $Cs_3Cu_2I_5$ for use in memristor-based transparent and flexible synapses. While we were studying transparent and flexible synapses using $Cs_3Cu_2I_5$, similar work using $Cs_3Cu_2I_5$ was reported for memristors and synapses,[24] which was however not applied to a transparent and flexible device. Moreover, the detailed mechanism was not studied.

Here, we report on a transparent and flexible memristor device based on an ITO/PEDOT:PSS/$Cs_3Cu_2I_5$/Au configuration for artificial synapses (ITO and PEDOT:PSS stand for indium-doped tin oxide and poly(3,4-ethylenedioxythiophene) polystyrene sulfonate, respectively). Upon a writing pulse, a resistance of 243 MΩ is measured, leading to an energy consumption of 10.48 aJ μm^{-2}, which in turn fulfils the minimum resistance required for parallel operation of 10^6 arrays. The structural, optical and electrical properties of the material and devices are investigated using X-ray diffraction (XRD), UV-vis spectroscopy, and ultraviolet photoelectron spectroscopy (UPS) in combination with density functional theory (DFT) calculation. Weight updates related to potentiation and depression are studied for flat and bent devices, which are used to simulate the recognition task from the MNIST (Modified National Institute of Standards and Technology) dataset.

Results and discussion

The crystal structure of the $Cs_3Cu_2I_5$ film deposited on the ITO substrate was investigated by XRD, as shown in Fig. 1(a). The XRD peaks were indexed to be orthorhombic phase and the lattice constants were estimated to be $a = 10.16570 \pm 0.0007$ Å, $b = 11.64140 \pm 0.0008$ Å and $c = 14.34972 \pm 0.0015$ Å, which is well consistent with the previous reports,[20–23] with space group of *Pnma* (ICSD ID: 150298 or CCDC ID: 1667479†).[25] The scanning electron microscope (SEM) image in Fig. 1(b) shows that the $Cs_3Cu_2I_5$ film is composed of *ca.* 110 nm-sized grains. The film thickness was determined to be about 290 nm as measured by a cross-sectional SEM image (Fig. S1, ESI†). The deposited film shows a highly transparent nature with an average transmittance of about 90% in the wavelength range from 500 nm to 900 nm (Fig. 1(c)). The optical bandgap of the $Cs_3Cu_2I_5$ film was determined to be 3.89 eV using an absorption spectrum and a direct-transition-based Tauc plot (Fig. S2, ESI†). This wide bandgap is responsible for the high transparency in the visible light region. Since low-temperature processing is beneficial to the deposition of polycrystalline $Cs_3Cu_2I_5$ on a polymer-based flexible substrate,[26] a flexible memristor device was facilely prepared by coating the $Cs_3Cu_2I_5$ film on the ITO-coated PET (polyethylene terephthalate, melting point >250 °C) substrate with a PEDOT:PSS buffer layer pre-coated on the ITO. The transparent and flexible memristor device structure is schematically presented in Fig. 1(d), where an Au electrode is deposited on the $Cs_3Cu_2I_5$ film. The Au top electrode and the ITO bottom electrode function like the presynaptic and postsynaptic terminals in biological systems,[27,28] such as an axon terminal and a dendrite in a biological neuron cell, as shown in Fig. 1(e). In a biological system, information in the form of an electric impulse is transmitted from the axon to the dendrite by the synaptic process. It is well known that the electric signal is transmitted by neurotransmitter release in the gap between the axon terminal and the dendrite, *via* calcium ion influx. In an artificial synapse, similar to the biological synaptic process, the electric signal is transmitted by vacancy or ion migration. The purpose of insertion of a PEDOT:PSS layer between the ITO and the $Cs_3Cu_2I_5$ is to prevent abrupt resistive switching due to an excessive conductance change.[28]

Resistive switching was investigated upon bending the flexible memristor device employing $Cs_3Cu_2I_5$. The device was bent at a bending radius of 5 mm, then the current–voltage (*I–V*) was measured. An abrupt SET at high voltage was observed when the positive voltage sweeps from 0 V to +6 V (Fig. S3, ESI†), where the SET process occurs at 5.4 V. A RESET process occurs at −2.2 V upon sweeping the negative voltage between 0 V and −3 V. A change from the high resistance state (HRS) to the low resistance state (LRS) occurs at SET process and the reverse is defined as the RESET process.[4,5,17] This memristive *I–V* characteristic can be applied to artificial synapses but a gradual analog resistive switching behavior is required for synaptic emulation.[7,17] Thus, to investigate analog resistive switching behavior, the positive voltage sweep from 0 V to +3 V and then back to 0 V, defined as one cycle, was repeated for five cycles and

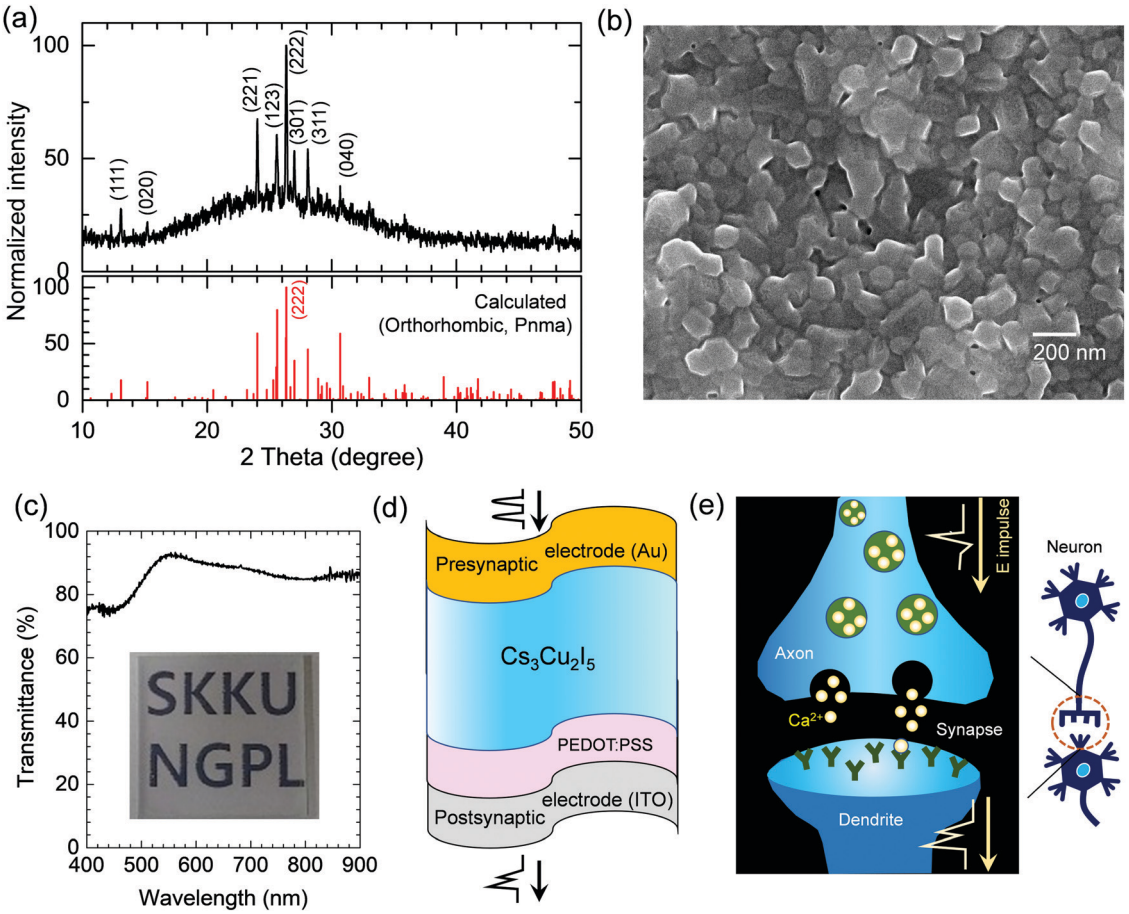

Fig. 1 (a) X-ray diffraction (XRD) pattern of the $Cs_3Cu_2I_5$ film on the ITO substrate. The calculated XRD pattern is based on orthorhombic $Cs_3Cu_2I_5$ with space group of *Pnma* corresponding to ICSD ID: 150298 (CCDC ID: 1667479†). (b) Scanning electron microscope (SEM) image and (c) transmission spectrum of the $Cs_3Cu_2I_5$ film. The inset image in (c) shows the see-through nature of the $Cs_3Cu_2I_5$ film. (d) Schematic illustration of the $Cs_3Cu_2I_5$-based flexible memristor device for artificial synapses. The Au electrode and the ITO electrode function as the presynaptic and postsynaptic electrodes, respectively. (e) Schematic illustration of a biological synapse composed of an axon (corresponding to the presynaptic terminal), a synaptic cleft and a dendrite (corresponding to the postsynaptic terminal). The right panel shows two neurons connected by a synapse.

the negative voltage sweep between 0 V and −3 V was performed for five cycles after the fifth positive voltage sweep cycle (Fig. 2(a)). The absolute current value gradually increased from the fifth to the fifth cycle at positive voltage, while it decreased from the sixth to tenth cycle at negative voltage. In order to investigate the cycle-to-cycle variability and repetition of the analog switching, 100 switching cycles for a given cell (Fig. S4, ESI†) and for different 50 cells (Fig. S5, ESI†) were repeatedly measured with a bent device. The ratio of standard deviation to average value was estimated to be 2.99% and 5.33% for LRS and HRS, respectively, for 100 cycles of the given single cell and 2.72% and 2.7% for the 50 different cells. This indicates that resistive switching in the bent device is highly reproducible.[29] Regarding the resistive switching mechanism in a memristor, there are two types: filamentary and interface.[30,31] The filamentary type originates from the formation of conductive filaments in the SET process, leading to LRS, and dissolution in the RESET process, resulting in HRS in the entire insulating layer, whereas the interface type occurs near the interface between the insulator and the electrode *via* the electric-field-induced modulation of the Schottky barrier. The portions of the active switching area in the top electrode that are filamentary and interface type can be distinguished because only areal switching is expected in the interface type as compared to current conductance in a narrow part in the filamentary type.[32] Thus, the different switching types can be distinguished by investigating the area dependence of the cell resistance (current). As shown in Fig. 2(b), the $Cs_3Cu_2I_5$-based memristor shows interface-type behavior because current is increased by 40 times as the active area is increased from 1.96×10^3 μm^2 to 1.25×10^5 μm^2 at each given bias voltage of 0.5 V, 1.0 V and 1.5 V. To investigate the origin of the resistive switching, we first studied the electrochemical impedance spectroscopy. The capacitance–frequency curve in Fig. 2(c), derived from the Nyquist plot in Fig. S6 (ESI†), shows that the capacitance reaches a plateau at frequencies higher than 100 Hz, whereas the capacitance is significantly increased at frequencies lower than 100 Hz. The constant capacitance at high frequency is probably related to the dielectric capacitance of $Cs_3Cu_2I_5$, while the increase in capacitance at low frequency is attributed to ion (most probably iodide anion) transport at the interface between

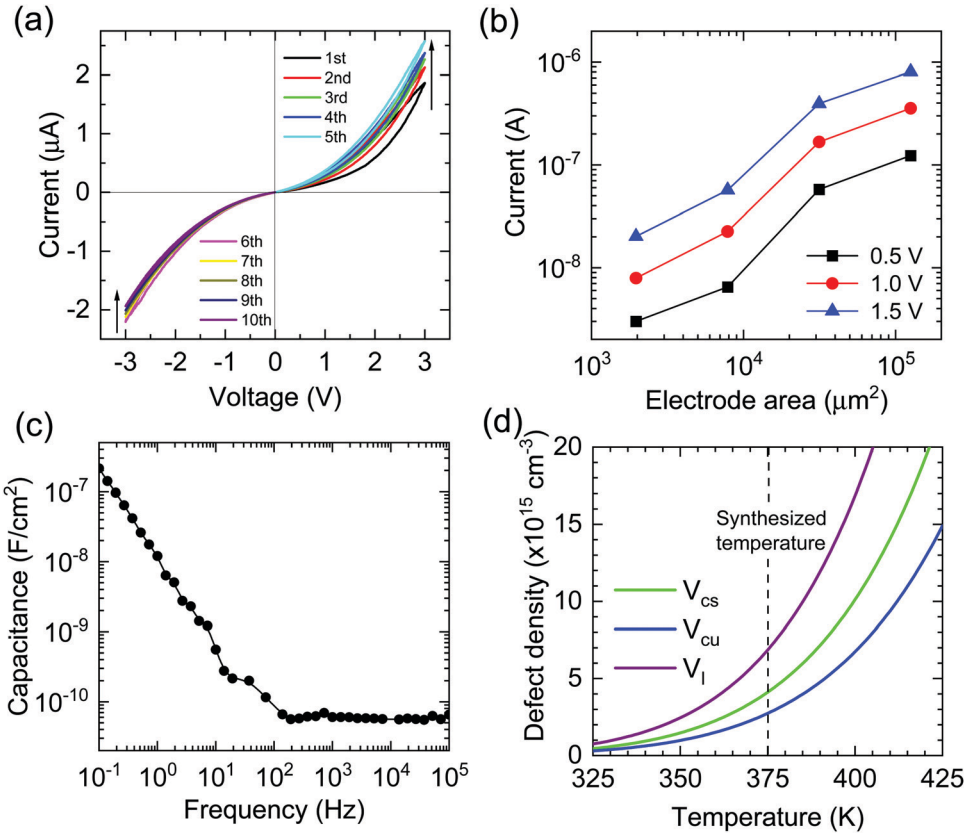

Fig. 2 (a) *I*–*V* curves of the flexible memristor device based on $Cs_3Cu_2I_5$, measured under bending with a radius of 5 mm. Positive voltage sweeps between 0 V and +3 V for five cycles (1st through 5th), which was followed by sweeping negative voltage from 0 V to −3 V for five cycles (6th through 10th). (b) Dependence of current on electrode area at applied voltages of 0.5 V, 1 V and 1.5 V. (c) Capacitance–frequency curve of the flexible memristor with an ITO/PEDOT:PSS/$Cs_3Cu_2I_5$/Au configuration. (d) Calculated defect density corresponding to equilibrium concentrations of Cs^+, Cu^+, and I^- vacancies (VCs, VCu and VI) as a function of temperature.

the $Cs_3Cu_2I_5$ and the electrode.[33,34] This underlines that ion (or vacancy) migration might be involved in modulating the Schottky barrier. To further investigate the origin of the change in conductance in the flexible $Cs_3Cu_2I_5$ memristor, we performed point defect simulations for all possible vacancies. Given the crystal symmetry of *Pnma*, there are two different Cs sites (Cs1 and Cs2), two different Cu sites (Cu1 and Cu2), and four I sites (I1, I2, I3, and I4), as shown in Fig. 3(a).[25] Under the assumption of stochiometric defect formation (Schottky disorder), the equilibrium defect concentration (n_d) was predicted by eqn (1):[35]

$$n_d = N_d \exp\left(\frac{-\Delta H_s}{k_B T}\right) \quad (1)$$

in which N_d is the lattice site concentration, ΔH_s is the Schottky defect energy, k_B is the Boltzmann constant, and T is the temperature. ΔH_s was calculated using the following reaction:[35]

$$\text{nil} \rightarrow 2V_{Cs1} + V_{Cs2} + V_{Cu1} + V_{Cu2} + V_{I1} + V_{I2} + 2V_{I3} + V_{I4} + Cs_3Cu_2I_5$$

where nil represents the lattice energy of $Cs_3Cu_2I_5$. ΔH_s was calculated to be 0.47 eV. The predicted equilibrium vacancy concentration of I is higher than that of Cs and Cu at our annealing temperature (373 K), at which the equilibrium vacancy concentrations of Cs, Cu and I are estimated to be 3.81×10^{15}, 2.54×10^{15}, and 6.35×10^{15} cm^{-3}, respectively (Fig. 2(d)).

Based on our defect models, we further performed nudged elastic band (NEB) calculations in order to predict the ion migration barriers of Cs^+, Cu^+, and I^-, assuming a vacancy-mediated ion migration mechanism. Owing to the low symmetry of the crystal structure, there are a number of accessible pathways for ion transport. For Cs migration, we considered two different Cs migration paths, which are Cs1–Cs2 and Cs1–Cs2′, as shown in Fig. 3(b), referring to the migration of a vacancy (V_{Cs}) from a Cs1 site to the nearest Cs2 site and to the second-nearest Cs2 site, respectively. Although the Cs1–Cs2 path has a much lower migration barrier (0.44 eV) than the Cs1–Cs2′ one (0.85 eV), it is not possible to construct a full Cs channel that penetrates the unit cell using only a Cs1–Cs2 connection. Therefore, forming a Cs channel with an alternate Cs1–Cs2 and Cs1–Cs2′ path is the minimum requirement for Cs ion migration in $Cs_3Cu_2I_5$. In Fig. 3(f), we plot a Cs channel that is composed of Cs1–Cs2 and Cs1–Cs2′ paths within the unit cell, along with fractional coordinates. Here, we note that the Cs1–Cs2 path is equivalent to the Cs1′–Cs2′ path and the Cs1–Cs2′ path is equivalent to the Cs1′–Cs2 path. For Cu migration, we modeled three different Cu migration paths, namely Cu1–Cu2, Cu1–Cu1′, and Cu2–Cu2′. The Cu1–Cu2 path defines the migration of a vacancy (V_{Cu}) from a

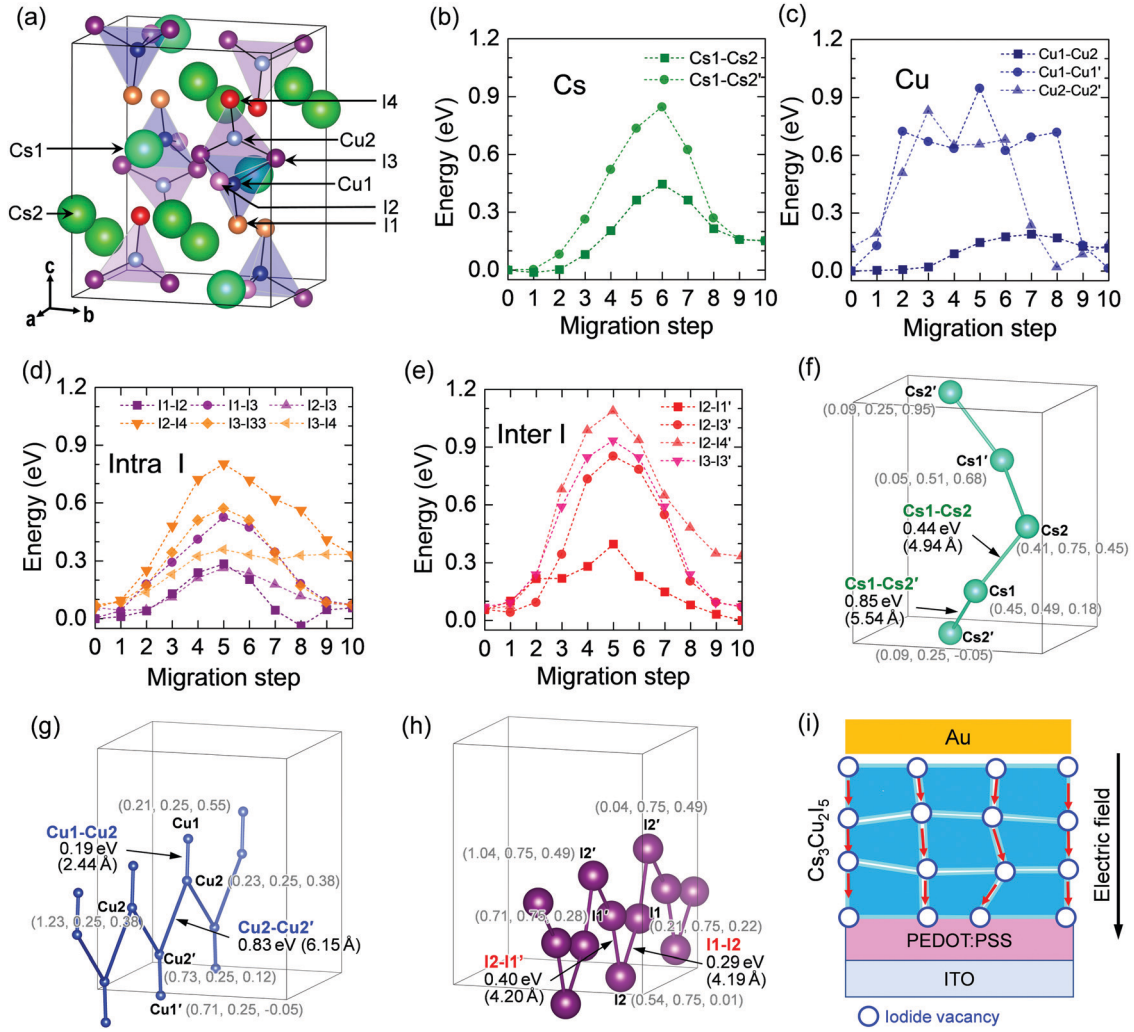

Fig. 3 (a) Atomic positions in the $Cs_3Cu_2I_5$ unit cell showing different Cs, Cu and I sites. Vacancy-mediated ion migration barriers of (b) Cs^+, (c) Cu^+ and (d) intra I^-, and (e) inter I^- depending on vacancy site pairs where the relative stabilities among different vacancy sites are reflected. Cs2 is the nearest Cs2 site to the Cs1 site and Cs2′ is the second-nearest Cs2 site to the Cs1 site. Cu1 and Cu2 sites are within the same $[Cu_2I_5]$ cluster while Cu1′ and Cu2′ represent Cu1 and Cu2 sites in the neighboring cluster. I1, I2, I3, and I4 represent I sites in the same cluster, whereas I1′, I3′, and I4′ are indicative of I sites in the neighboring cluster. Visualization of ion migration channels of (f) Cs^+, (g) Cu^+ and (h) I^-, where each channel is constructed by combining the low energy barrier paths in (b), (c), (d), and (e). Namely, (f) shows the Cs ion migration channel, which is composed of Cs1–Cs2 and Cs1–Cs2′ paths, where the Cs1–Cs2 and Cs1–Cs2′ paths are equivalent to the Cs1′–Cs2′ and Cs1′–Cs2 paths, respectively. (g) Cu ion migration channel, which is composed of Cu1–Cu2 and Cu2–Cu2′ paths, where the Cu1–Cu2 path is equivalent to the Cu1′–Cu2′ path. (h) I ion migration channel, which is composed of I1–I2 and I2–I1′ paths where the I1–I2 and I2–I1′ paths are equivalent to the I1′–I2′ and I2′–I1 paths, respectively. Paths including I3 and I4 are not shown in (h) since they have higher migration barriers than the other paths. For each element site, the fractional coordinates within the unit cell are annotated in parentheses. For each migration path, the migration barrier (in unit of eV) and path length (in unit of Å) are annotated. (i) Schematic illustration of migration of iodide vacancy in the $Cs_3Cu_2I_5$ layer when an electric field is applied.

Cu1 site to a Cu2 site within a $[Cu_2I_5]^{3-}$ cluster (two iodides (I3) are shared, see Fig. 3(a) for details), while the Cu1–Cu1′ (Cu2–Cu2′) path is indicative of the migration of a vacancy from a Cu1 (Cu2) site to a Cu1 (Cu2) site in the neighboring $[Cu_2I_5]^{3-}$ cluster. Even though the Cu1–Cu2 path has the lowest migration barrier of 0.19 eV, this path cannot lead to the formation of a Cu channel that penetrates the unit cell because it is confined within a single cluster. Since the Cu2–Cu2′ path has lower barrier (0.83 eV) than the Cu1–Cu1′ path (0.95 eV) (Fig. 3(c)), ion migration through the Cu2–Cu2′ path can dominate, as shown in Fig. 3(g). It is noted that the Cu1–Cu2 path is equivalent to the Cu1′–Cu2′ path. Finally, iodide migration was investigated, where six intra-cluster I migration paths and four inter-cluster I migration paths were considered. Fig. 3(d and e) show the calculated energies for the intra- and inter-cluster I migration paths, where I1, I2, I3, and I4 are I sites within the same $[Cu_2I_5]^{3-}$ cluster while I1′, I3′, and I4′ represent I sites in the nearest neighboring cluster. Among intra-cluster I migration paths, the I1–I2 and I2–I3 paths were found to have lower migration barriers (<0.3 eV) than the other paths, while the I2–I1′ path is estimated to have the lowest migration barrier (0.40 eV) among the inter-cluster I migration paths. In order for the iodide vacancies (V_Is) to run through the

unit cell, a combination of intra- and inter-cluster migration paths is required. We confirm that the combination of I1–I2 and I2–I1′ paths can construct an I channel that penetrates the unit cell, which is illustrated in Fig. 3(h), where the I1–I2 path is equivalent to the I1′–I2′ path and the I2–I1′ path is equivalent to the I2′–I1 path. Combinations of other paths, such as an alternative I3–I3 and I3–I3′ path, can be possible as channels for iodide migration penetrating the unit cell, but their energy barriers are much larger than those of the I1–I2 and I2–I1′ paths. Since the lowest barriers for the Cs and Cu channels are two times larger than that of the I channel, the most probable I channel is determined to be the I2–I1′ path with a barrier of 0.40 eV. The migration of an iodide vacancy in a $Cs_3Cu_2I_5$ layer is thus proposed to be responsible for the resistive switching, as illustrated in Fig. 3(h).

Under the premise of the probable change in valence state of Cu at the interface of $Cs_3Cu_2I_5$ layer owing to the migration of iodide vacancies, we investigated the electrical conduction mechanism using a natural logarithmic *I–V* curve in a single sweep. Current linearly increased with bias voltage at low electric field (applied voltage <0.25 V ($\ln 0.25$ V $= -1.39$ V)), while non-linearity between *I* and *V* was observed at high electric field (applied voltage >0.25 V) (Fig. 4(a)), which indicates that two different conduction mechanisms are involved. The slope of $\ln I/\ln V$ at voltage lower than 0.25 V was determined to be 1.09 and 1.07 for the HRS and LRS, respectively, which is indicative of ohmic conduction occurring at low electric field.[4,10] For bias voltages larger than 0.25 V, deviation from linearity underlines a different conduction mechanism. Since most halide perovskite materials reported for memristors exhibit Schottky conduction, the current is plotted with respect to $V^{1/2}$ at high electric field for both HRS and LRS because logarithmic current is expected to be proportional to the square root of bias voltage according to eqn (2):[10,36]

$$I = AT^2 e\left[\frac{-q\left(\phi_B - \sqrt{\frac{qV}{4\pi\varepsilon_r\varepsilon_0}}\right)}{kT}\right] \quad (2)$$

where *I* is the current, *A* is Richardson's constant, *T* is the absolute temperature, *q* is the elementary charge, ϕ_B is the Schottky barrier height, *V* is the bias voltage, ε is the dielectric permittivity (ε_0 is vacuum permittivity) and *k* is Boltzmann's constant. The *I–V* curve well fitted a linear line for both HRS and LRS at high electric field, giving rise to high slopes of 3.97 for HRS and 3.92 for LRS (Fig. 4(b)). Furthermore, the temperature-dependent current, represented by $\ln I/T^2$ *versus* $1/T$ in Fig. 4(c), shows a linear relationship, supporting Schottky conduction. Since both ohmic conduction and thermionic conduction are probably related to the electronic band structure and dynamics of the charge carriers, density functional theory (DFT) calculation and ultraviolet photoelectron spectroscopy (UPS) measurement were carried out. $Cs_3Cu_2I_5$ has a dispersive lower conduction band and a flat valence band (Fig. 4(d)). There is a direct bandgap of 3.82 eV calculated at the Γ-point, which is slightly lower but very close to the bandgap of 3.89 eV obtained from the Tauc plot in Fig. S2 (ESI†). To analyze the dynamics of

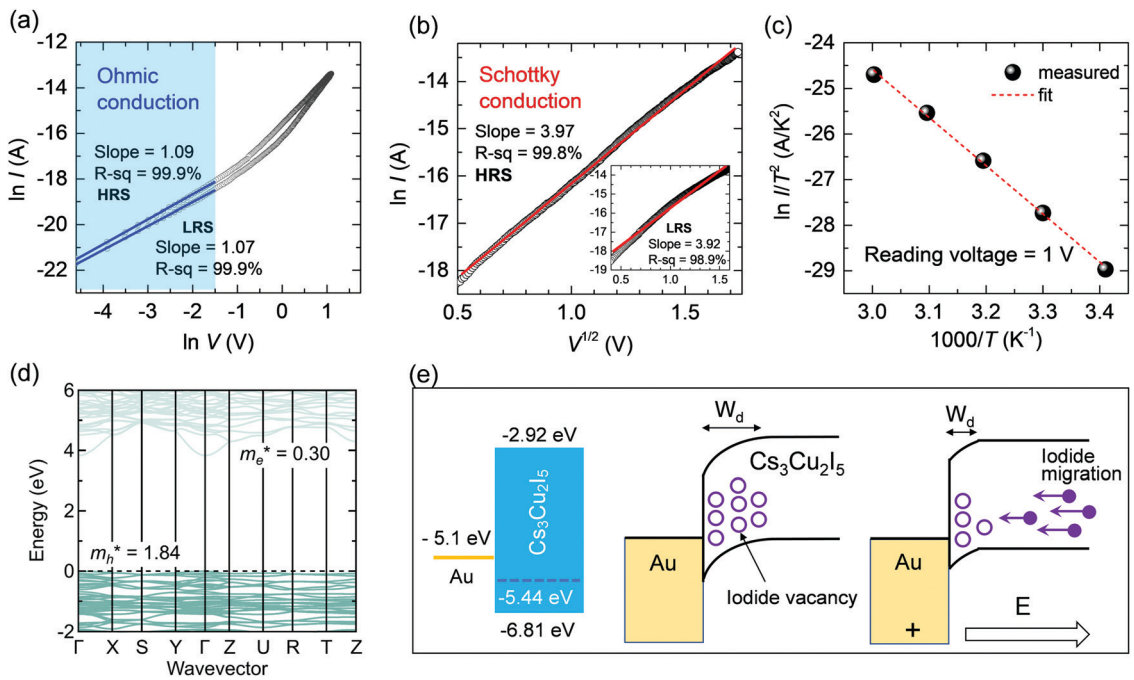

Fig. 4 (a) Natural logarithmic *I–V* plots and linear fit results at low voltage in a single sweep. (b) $\ln I$ *versus* $V^{1/2}$ plot at HRS and LRS (inset) and linear fit result. (c) $\ln(I/T^2)$ *versus* $1000/T$ in HRS of single sweep measured at 1 V. (d) Electronic band structure of $Cs_3Cu_2I_5$ within the HSE06 level of theory. VBM is set as 0 eV and m_e^* and m_h^* denote the effective masses of an electron and a hole, respectively, in units of m_e. (e) CBM, VBM and work function of $Cs_3Cu_2I_5$. Schottky junction between p-type $Cs_3Cu_2I_5$ and Au at equilibrium and under electric field, showing the change in the depletion layer width, W_d.

charge carriers affecting current flow, effective masses were calculated using the finite difference method, where additional k-points are sampled around the band extrema to derive the $\frac{d^2E}{dk^2}$ tensor. The effective masses of an electron (m_e^*) and a hole (m_h^*) are estimated to be 0.30 m_e and 1.84 m_e, respectively. This asymmetric carrier transport (*i.e.*, small electron effective mass and large hole effective mass) is a unique property of $Cs_3Cu_2I_5$, which has not been observed in conventional lead-based low-dimensional metal halides such as Cs_4PbBr_6[37]. From the UPS measurements in Fig. S7 (ESI†), the binding energies of the valence band (E_{vb}) and cut-off ($E_{cut\text{-}off}$) were evaluated to be 1.37 eV and 15.76 eV, respectively. The valence band maximum (VBM) was calculated according to $|VBM| = h\nu - E_{cut\text{-}off} + E_{vb}$, where $|h\nu - E_{cut\text{-}off}|$ corresponds to the work function.[38] As we used a He (I) (21.2 eV) source, the VBM and CBM were found to be −6.81 eV and −2.92 eV, respectively, along with a work function of −5.44 eV, indicative of p-type characteristic. As can be seen in Fig. 4(e), the flat band of the p-type $Cs_3Cu_2I_5$ is depleted by the Schottky junction with Au (work function of −5.10 eV). It was reported that the depletion layer width (W_d) could change with vacancy concentration in interface-type resistive switching.[39] In the case of interface-type resistive switching based on a p-type semiconductor, the electric field generated by a positive voltage bias on the top electrode decreases W_d between the top electrode and the switching medium by migration of anion vacancies to the bottom electrode, which increases the current of memristor devices.[39] Based on this phenomenon and our calculation results for ion migration in p-type $Cs_3Cu_2I_5$ memristor devices, the W_d of $Cs_3Cu_2I_5$ is decreased because the iodide vacancies at the interfcae are reduced by vacancy migration from the top Au electrode to the bottom ITO electrode (or iodide migration from ITO to Au) under the electric field generated by a positive voltage bias on the Au electrode, as expected in Fig. 3(i), which leads to an increase in current.

Based on the analyzed electrical conduction mechanism, we investigated the synaptic properties of the flexible $Cs_3Cu_2I_5$ memristor with a bending radius of 5 mm. Although $Cs_3Cu_2I_5$ is a p-type semiconductor and exhibits interface type resistive switching by migration of iodide vacancies, the migration of holes in the $Cs_3Cu_2I_5$ layer is expected to be slow because of the much larger effective mass of holes (1.84 m_e) as compared to other halide perovskite materials with effective hole mass of about 0.5 m_e.[40] This poor migration of charge carriers can affect the synaptic behavior of our memristor device. When a 500 μs pulse of 0.1 V is applied to the memristor device, the current is increased from 0.197 nA to 0.242 nA and then decayed to 0.199 nA, which results in a change in the synaptic weight (ΔG) of +1.01%, calculated by $(I_{final} - I_{initial})/I_{initial}$ (Fig. 5(a)).[4] This change is indicative of an excitatory postsynaptic current (EPSC) due to a partial migration of iodide vacancies in a $Cs_3Cu_2I_5$ layer from $Cs_3Cu_2I_5$ to the bottom PEDOT:PSS/ITO electrode. Fig. S8 (ESI†) exhibits a peak current at a +0.1 V pulse. Energy consumption is estimated to be 10.48 aJ μm^{-2} from a peak current of 0.411 nA under a 500 μs pulse at 0.1 V

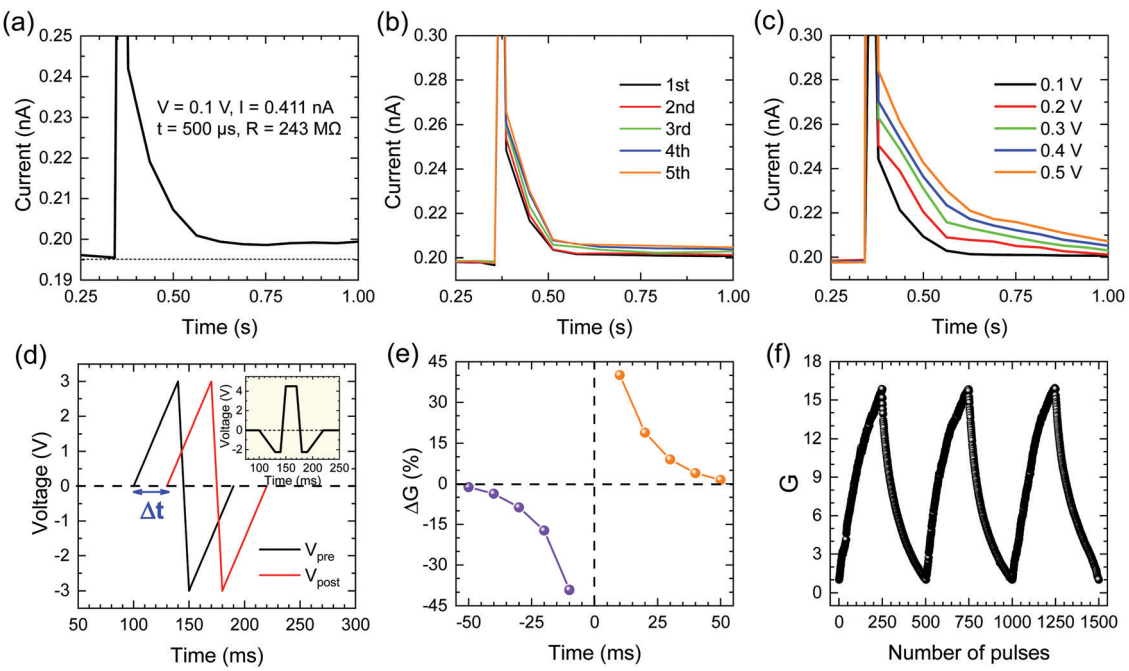

Fig. 5 Synaptic behavior of the $Cs_3Cu_2I_5$ flexible memristor with a bending radius of 5 mm. (a) EPSC characteristics observed at a 500 μs pulse of 0.1 V. A full current–time profile is presented in Fig. S8 (ESI†). (b) SNDP measured by applying a 500 μs pulse of 0.1 V five times. (c) SVDP observed at 500 μs pulses of 0.1 V, 0.2 V, 0.3 V, 0.4 V and 0.5 V. (d) Voltage of presynaptic and postsynaptic spikes over time for emulating STDP. (e) STDP behavior. ΔG stands for change of relative conductance. (f) Potentiation and depression depending on the number of pulses, where 250 consecutive positive pulses (2.5 V, 700 μs) for potentiation were followed by 250 negative pulses (−1 V, 700 μs) for depression. A 0.1 V reading voltage was applied after each positive and negative pulse. Potentiation and depression were repeated three times. G stands for relative conductance.

and an electrode area with radius of 25 μm (energy/area = 0.411 nA × 0.1 V × 500 μs/(π × 25 × 25 μm^2) = 20.55 fJ 1960 μm^{-2}).[4,17] This aJ μm^{-2}-scale low energy consumption is due to the relatively low current (0.411 nA) and high resistance (243 MΩ) caused by the aforementioned poor migration of charge carriers in $Cs_3Cu_2I_5$. Since the thickness of the switching layer is critical and its effect on current and resistance cannot be ruled out in memristive devices, we fabricated flexible memristor devices employing 190 nm-, 240 nm-, 290 nm- and 340 nm-thick $Cs_3Cu_2I_5$ films (Fig. S9, ESI†), where the film thickness is controlled by changing the concentration of the precursor solution.[41] By measuring EPSC with 0.1 V and 0.5 V pulses, we confirmed that the thickness of the $Cs_3Cu_2I_5$ film has little influence on the current and resistance of the flexible $Cs_3Cu_2I_5$ memristor (Fig. S10, ESI†). It was reported that the current of memristor devices based on other halide perovskite materials was minimally dependent on the thickness of the perovskite layer.[13,15] Thus, the energy consumption of the flexible $Cs_3Cu_2I_5$ memristor does not seem to be affected by the thickness of the $Cs_3Cu_2I_5$ film.

The resistance of 243 MΩ is higher than the minimum resistance required for parallel operation of over 10^6 arrays.[9] The scalability of arrays is affected by the resistance of memristor devices because voltage drops on the wire connection decrease the real voltage applied to synaptic devices such that the wire resistance reaches the resistance of a nanoscale device.[9,42] For these reasons, $Cs_3Cu_2I_5$ has potential for parallel operation of large-scale crossbar arrays composed of 1selector–1memristor (1S1M) or 1transistor–1memristor (1T1M). Moreover, the energy consumption of the $Cs_3Cu_2I_5$-based memristive device is the lowest among the studied materials (Table 1). We also confirm that ΔG increases from +1.01% to +1.56%, +2.42%, +2.78% and +3.33% when the number of pulses applied is increased to 2, 3, 4 and 5, respectively (Fig. 5(b) and Fig. S11, ESI†), which indicates that repetitive pulses of 0.1 V can increase the amount of iodide vacancies migrated to the interface between the $Cs_3Cu_2I_5$ and the PEDOT:PSS layer. This phenomenon is called spike-number-dependent plasticity (SNDP) and it is similar to the increase in plasticity in biological synapses when small stimuli are repeated.[40,43] Furthermore, ΔG increased from +1.01% to +1.51%, +2.25%, +3.38% and +4.44% when the voltage of pulses applied was increased to 0.2, 0.3, 0.4 and 0.5 V, respectively (Fig. 5(c) and Fig. S12, ESI†). This indicates that strong pulses can increase the amount of iodide vacancies at the interface between the $Cs_3Cu_2I_5$ and the PEDOT:PSS layer, which is called spike-voltage-dependent plasticity (SVDP).[43] SVDP is similar to the change in plasticity in biological synapses when the strength of stimulation is changed.[43] Moreover, energy consumption of the SNDP for the 2nd, 3rd, 4th and 5th pulses is 10.65, 10.71, 10.80 and 10.93 aJ μm^{-2}, respectively, and the energy consumption of the SVDP for 0.2 V, 0.3 V, 0.4 V and 0.5 V pulses is estimated to be 40.66, 84.57, 163.2 and 279.7 aJ μm^{-2}, respectively. Such low energy consumption values of less than 1 fJ μm^{-2} are highly viable for synaptic emulation. In addition to realizing low energy consumption, emulating spike-time-dependent plasticity (STDP) is important in artificial synapses. STDP means that the synaptic weight is determined by the time interval of the spikes between the presynaptic and postsynaptic terminals.[44,45] To mimic STDP in the flexible $Cs_3Cu_2I_5$ memristor, two spikes of the same type with a specific time interval are required, as shown in Fig. 5(d), where one spike is applied to the top electrode (postsynaptic terminal) and the other is applied to the bottom electrode (presynaptic terminal).[44,45] The time interval between spikes applied to the top electrode and the bottom electrode is defined as Δt ($\Delta t = t_{post} - t_{pre}$),[44,45] where two spikes are converted into one net spike to realize STDP in the flexible $Cs_3Cu_2I_5$ memristor device (see inset in Fig. 5(d)).[46,47] If the postsynaptic spike arrives after the presynaptic spike ($\Delta t > 0$), the net polarity of the spikes is positive and the synaptic weight is potentiated ($\Delta G > 0$).[44–47] On the other hand, when the presynaptic spike arrives later than

Table 1 Comparison of the resistance for the writing pulse and the energy consumption of $Cs_3Cu_2I_5$ with other materials

Materials	Specific property[d]	Resistance for a writing pulse	Energy consumption (cell area)	Ref.
$MAPbI_3$		366.6 Ω	5500 fJ μm^{-2} (0.06 cm^2)	49
$MA_3Sb_2Br_9$		1.34×10^3 Ω	118 fJ μm^{-2} (7853 μm^2)	4
$MAPbBr_3$		$\sim 3.33 \times 10^5$ Ω	34.5 fJ μm^{-2} (12 mm^2)	17
$FAPbBr_3$		$\sim 1.42 \times 10^5$ Ω	23 fJ μm^{-2} (12 mm^2)	17
$CsPbBr_3$		$\sim 2.0 \times 10^4$ Ω	123 fJ μm^{-2} (12 mm^2)	17
PEA_2PbBr_4		2.5×10^{10} Ω	400 fJ μm^{-2} (1 μm^2)	40
MoS_2/h-BN[a]		3.3×10^7 Ω	60.0 aJ μm^{-2} (300 μm^2)	50
$Hf_{0.5}Zn_{0.5}O$	F	$\sim 2.5 \times 10^4$ Ω	1.6×10^7 fJ μm^{-2} (1000 μm^2)	51
pPPI[a]	F	4.46×10^3 Ω	2.49×10^3 fJ μm^{-2} (225 μm^2)	52
C_{60}	F	$< 1.60 \times 10^6$ Ω	2.0×10^5 fJ μm^{-2}(1000 μm^2)	53
PEI,PEDOT:PSS	F/T	1.61×10^5 Ω	10 fJ μm^{-2} (1000 μm^2)	28
PEDOT:PSS	F/T	$\sim 1.67 \times 10^7$ Ω	214.9 fJ μm^{-2} (31 415 μm^2)	54
PEDOT:PSS	F/T	1.97×10^8 Ω	8.04 fJ μm^{-2} (31 415 μm^2)	55
PDADMAC[b]	F/T	5.0×10^3 Ω	5.0 fJ μm^{-2} (40 000 μm^2)	56
Collagen	F/T	1.66×10^5 Ω	5.0×10^5 fJ μm^{-2} (10 000 μm^2)	57
In_2O_3	F/T	$\sim 2.0 \times 10^4$ Ω	666.7 fJ μm^{-2} (1.5×10^5 μm^2)	58
CtC[c]	F/T	2.0×10^3 Ω	1273 fJ μm^{-2} (7853 μm^2)	59
ZnO	F/T	3.5×10^3 Ω	580 fJ μm^{-2} (70 685 μm^2)	7
$Cs_3Cu_2I_5$	**F/T**	**2.4×10^8 Ω**	**10.48 aJ μm^{-2} (1960 μm^2)**	**This work**

[a] 1-Phenyl-2-(4-(pyren-1-yl)phenyl)-1*H*-phenanthro[9,10-*d*]imidazole. [b] Polydiallyldimethylammonium chloride. [c] Carboxymethyl iota-carrageenan. [d] F: flexible, T: transparent.

the postsynaptic spike, the net polarity of the spikes is negative and the synaptic weight is depressed ($\Delta G < 0$).[44–47] ΔG is negatively dependent on the time interval between the presynaptic and postsynaptic spikes, which means that the absolute value of synaptic weight increases as Δt gets closer to 0 (Fig. 5(e)). This behavior indicates that the STDP of biological synapses is well emulated in the flexible $Cs_3Cu_2I_5$ memristor. To investigate the weight update, 250 pulses of 2.5 V and −1 V were applied for potentiation and depression, respectively, where the reading voltage is 0.1 V. As shown in Fig. 5(f), linear potentiation and depression are realized with an almost invariant dynamic range (relative conductance) of 15.85, 15.84 and 15.86, where the ratio of the standard deviation to the average value is estimated to be 5.98% and no abrupt change of synaptic weight is observed. Moreover, the synaptic weight is well retained at 50, 100, 150, 200 and 250 pulses for over 50 s (Fig. S13, ESI†), which corresponds to the long-term plasticity (LTP) of biological synapses.[48]

To investigate changes to the synaptic weight updates depending on the bending condition, potentiation and depression were evaluated for several bending conditions (Fig. 6(a)), where +2.5 V and −1 V were chosen for potentiation and depression, respectively. As compared to the dynamic range of 15.6 for the flat state without bending, the bent device and the device after 100 bending cycles (recovered) show similar dynamic ranges of 16.3 and 15.1 without any abrupt change in the weight updates for 250 potentiations and depressions, which indicates that this flexible memristor can be applied to pattern recognition tasks based on ANNs even under bent state without pulse modulation technique.[28,48,60,61] We also investigated weight updates depending on the bending radius and substrate type (glass substrate *vs.* flexible substrate). The potentiation and depression characteristics for the $Cs_3Cu_2I_5$ film deposited on a rigid glass substrate are almost identical to those for the film on a PET substrate (Fig. S14, ESI†). This indicates that the synaptic emulation of the $Cs_3Cu_2I_5$ memristor is hardly affected by the substrate. When the bending radius (R) is changed from 5 mm to 7 mm, the dynamic range for the linear potentiation and depression is marginally changed from 15.78 to 16.28, which are similar to the flat state (15.60) (Fig. S15, ESI†). However, the behavior becomes totally different when the bending radius is reduced to 3 mm, which might be owing to the film morphology of $Cs_3Cu_2I_5$ with pinholes at the $Cs_3Cu_2I_5$–substrate interface (see Fig. S1, ESI†). This could be solved by forming a pinhole-free and higher quality morphology using various deposition methods.[62–64] In addition to the weight update behavior depending on bending radius, the maximum and intermediate conductance states were well retained for over 50 s for all bending conditions of the $Cs_3Cu_2I_5$ flexible memristor (Fig. 6(b)), which indicate that LTP is well realized for all bending conditions. Furthermore, as shown in Fig. 6(c), the energy consumption required for the maximum conductance (G_{max}) is ~100 pJ μm^{-2} for $Cs_3Cu_2I_5$, which is one order of magnitude lower than that required for $MAPbI_3$ (~1 nJ μm^{-2}).[49] With weight updates related to potentiation and depression, we

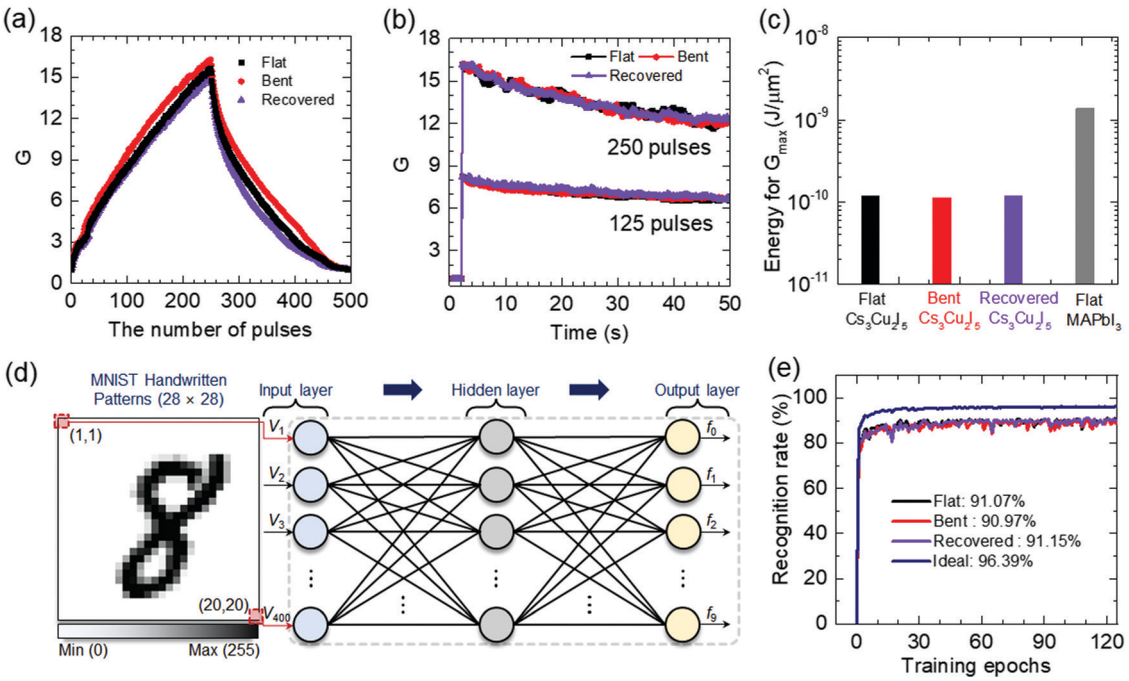

Fig. 6 Characteristics of $Cs_3Cu_2I_5$-based memristor devices related to ANNs depending on bending condition. (a) Potentiation and depression depending on the number of pulses, where 250 consecutive positive pulses (2.5 V, 700 μs) for potentiation were followed by 250 negative pulses (−1 V, 700 μs) for depression. A 0.1 V reading voltage was applied after each positive and negative pulse. (b) LTP based on the number of pulses. (c) Energy consumption of the flat, bent and recovered devices required for 250 conductance states, where flat $MAPbI_3$ was selected as a comparative material. (d) MNIST handwritten patterns composed of 784 pixels and ANNs based on multilayer perceptron model. (e) Recognition rate for flat, bent, and recovered devices as a function of the number of training epochs. Value for ideal means the maximum obtainable from the software.

simulated pattern recognition tasks based on ANNs, where a multilayer perceptron (MLP) algorithm comprising a three-layer neural network with 784 (28 × 28) pre-neurons, hidden neurons and 10 output neurons was utilized to learn a MNIST handwritten pattern dataset (Fig. 6(d)).[30,55] The 784 neurons of the input layer correspond to a MNIST handwritten pattern of 784 pixels and the 10 neurons of the output layer correspond to 10 classes of digits (0–9). The MNIST image data (V_1–V_{784}, V) is transmitted as the input signal for the 1st layer of neurons.[30,55] Then, the inner product of the input vector signal for the 1st layer neurons is summed, which is used as the input of the hidden layer. After the activation process by using a sigmoid function, the change in the synaptic weight was calculated, which provides feedback to adjust the synaptic weights through comparing the real output to the target output. After one million patterns randomly chosen from 60 000 images of a training set are trained, the recognition rate was tested with a separate set of 10 000 images of the testing set. Recognition rates in flat, bent and recovered states were estimated to be 91.07%, 90.97% and 91.15% without pulse modulation technique, respectively, when an ideal recognition rate of software is 96.39% (Fig. 6(e)). Our recognition rate is comparable with those for other memristor devices that exploit the pulse modulation technique for recognition rates over 90%.[60,61] This indicates that $Cs_3Cu_2I_5$ is highly suitable for flexible artificial synapses because of the independence of the synaptic behavior from bending.

Conclusion

Sub-femtojoule energy consumption transparent and flexible artificial synapses were developed based on the thin film of p-type $Cs_3Cu_2I_5$. Interface-type resistive switching was verified from the device with the configuration of Au/$Cs_3Cu_2I_5$/PEDOT:PSS/ITO. The migration of iodide vacancies and the asymmetric carrier transport of $Cs_3Cu_2I_5$ were found to play important roles in establishing the high resistance to realize low energy consumption, which has potential for use in scalable neuromorphic computing. It is noted that the synaptic weight updates related to potentiation and depression were hardly changed by bending, which is highly beneficial for flexible optoelectronics that require artificial synapses.

Conflicts of interest

The authors declare no conflict of interest.

Acknowledgements

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